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| Name: Zain Akhtar | EE-272L Digital Systems Design |
| Reg. No.:2023-EE-63 | Marks Obtained: \_\_\_\_\_\_\_\_\_\_\_\_ |

Lab Manual

Experiment 3: Combinational Circuits Design Using Vivado

DSD Lab Manual Evaluation Rubrics

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Assessment | Total  Marks | Marks Obtained | 0-30% | 30-60% | 70-100% |
| Code  Organization  (CLO1) | 3 |  | No Proper Indentation and descriptive naming, no code organization.    Zero to Some understanding but not working | Proper  Indentation or descriptive naming or code organization.    Mild to Complete understanding but not working | Proper  Indentation and descriptive naming, code organization.    Complete understanding, and proper working |
| Simulation  (CLO2) | 5 |  | Simulation not done or incorrect, without any understanding of waveforms | Working simulation with errors, don't cares's(x) and high impedance(z), partial understanding of waveforms | Working simulation without any  errors, etc and complete understanding of waveforms |
| FPGA  (CLO2) | 2 |  | Not implemented on FPGA and  questions related to synthesis and implementation not answered. | Correctly  Implemented on FPGA or  questions related to synthesis and implementation answered. | Correctly  Implemented on FPGA and  questions related to synthesis and implementation answered. |

# (a) Truth Table

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| a | b | c | ~c | a|b | ~(a&b) | ~(a&b)^(a|b) | x=(~c)^(a|b) | y=(a|b)&(~(a&b))^(a|b) |
| 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 |
| 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 |

# (b)Errors found in code

In listing 4

1. At line 6 (,) after carry
2. At line 9 assign is missing with sum
3. At line 10 and operator is missing (c(a^b))

In listing 5

1. At line 6 logic carry1 is missing
2. At line 7 instant is not created just module is called
3. In line 18 to 34 a1,b1,c1 should be used
4. At line 35 end is missing
5. At the end $monitor section is missing

# (c)Corrected codes

**For listing 4**

module full\_adder(

input logic a,

input logic b,

input logic c,

output logic sum,

output logic carry

);

assign sum = (a ^ b) ^ c;

assign carry = (a & b) | (c&(a ^ b));

endmodule

**For listing 5**

module full\_adder\_tb();

logic a1;

logic b1;

logic c1;

logic sum1;

logic carry1;

full\_adder lab3(

.a(a1),

.b(b1),

.c(c1),

.sum(sum1),

.carry(carry1)

);

initial

begin

// Provide different combinations of the inputs to check validity of code

a1 = 0; b1 = 0; c1 = 0;

#10;

a1 = 0; b1 = 0; c1 = 1;

#10;

a1 = 0; b1 = 1; c1 = 0;

#10;

a1 = 0; b1 = 1; c1 = 1;

#10;

a1 = 1; b1 = 0; c1 = 0;

#10;

a1 = 1; b1 = 0; c1 = 1;

#10;

a1 = 1; b1 = 1; c1 = 0;

#10;

a1 = 1; b1 = 1; c1 = 1;

#10;

$stop;

end

initial begin

$monitor("a=%b,b=%b,c=%b,sum=%b,carry=%b",a1,b1,c1,sum1,carry1);

end

endmodule